LISTING OF THE CLAIMS:

The claims remain as follows:

1. (Previously Presented) A pipelined circuit apparatus for performing operations on a first binary number and a second binary number, comprising:

a first arithmetic logic unit (ALU) operating on a first lower portion of the first binary number and a second lower portion of the second binary number to produce a first result and a carry out signal; and

a second ALU operating on a first upper portion of the first binary number and a second upper portion of the second binary number to produce a second result;

wherein at least one stage in the pipelined circuit stalls by one or more clock cycles in response to the carry out signal to account for additional delay introduced by incrementing the second result when the carry out signal indicates a carry.

2. (Original) The apparatus of claim 1 further comprising:

a memory having a first memory portion receiving the first result and a second memory portion receiving the second result.

3. (Previously Presented) The apparatus of claim 2 further comprising:

a logic circuit for incrementing a value stored in the second memory portion when the carry out signal indicates a carry.

4. (Original) The apparatus of claim 3 wherein:

the incremented value is stored into the second memory portion in response to the carry out signal.

5. (Original) The apparatus of claim 2 wherein:

the second memory portion is configured to increment a value stored in the second memory portion in response to the carry out signal.

6. (Original) The apparatus of claim 2 wherein:

the memory stores a value used to address a random access memory.

7. (Original) The apparatus of claim 1 wherein:

the first binary number is split in two at a first bit boundary to form the first upper portion and the first lower portion; and

the second binary number is split in two at a second bit boundary to form the second upper portion and the second lower portion.

8. (Original) The apparatus of claim 1 wherein:

the first binary number is associated with a first flag bit, the first flag bit indicating a first predetermined number of most significant bits of the first binary number are all zero;

the second binary number is associated with a second flag bit, the second flag bit indicating a second predetermined number of most significant bits of the second binary number are all zero; and

the apparatus further comprising:

a logic circuit selecting one of the first upper portion and the second upper portion in response to the first flag bit and the second flag bit, the selected upper portion used as the second result.

9. (Original) The apparatus of claim 8 further comprising:

at least two buffers for each bit position in the second result, each the buffer receiving a corresponding bit value within the second result, each the buffer driving an electrically conductive line that has minimum width.

10. (Original) The apparatus of claim 1 wherein:

the second binary number is split in two at a second bit boundary to form the second upper portion and the second lower portion.

11. (Previously Presented) A pipelined circuit apparatus, comprising:

an arithmetic logic unit (ALU) operating on two binary numbers, the ALU comprising:

a first logic circuit generating a carry out signal from a bit location that is not the most significant bit of the ALU;

wherein at least one stage of the pipelined circuit stalls by one or more clock cycles in response to the carry out signal to account for additional delay introduced by incrementing the second result when the carry out signal indicates a carry.

12. (Original) The apparatus of claim 11, the ALU further comprising:

a first logic unit operating on lower portions of the two binary numbers to produce a first result;

a second logic unit operating on upper portions of the two binary numbers to produce a second result;

a second logic circuit for incrementing the second result in response to the carry out signal to form an incremented value.

13. (Original) The apparatus of claim 12 wherein:

a final result for the ALU is formed by combining:

the first result, and

selection of one of the second result and the incremented value, the selection being done in response to the carry out signal.

14. (Original) The apparatus of claim 12, the ALU further comprising:

a first memory storing the first result; and

a second memory conditionally storing either the second result or the incremented value, the condition determined in response to the carry out signal.

15. (Original) The apparatus of claim 11 wherein:

a first flag bit is associated with a first of the two binary numbers, the first flag bit indicating a predetermined number of most significant bits of the first binary number are all zero;

a second flag bit is associated with a second of the two binary numbers, the second flag bit indicating a predetermined number of most significant bits of the second binary number are all zero;

the apparatus further comprising:

a logic circuit selecting an upper portion of one of the two binary numbers, the selecting done in response to the first flag bit and the second flag bit;

16-17. (Cancel)

18. (Previously Presented) An integrated circuit comprising a pipelined circuit for performing operations on a first binary number and a second binary number, the pipelined circuit comprising:

a first arithmetic logic unit (ALU) operating on a first lower portion of the first binary number and a second lower portion of the second binary number to produce a first result and a carry out signal; and

a second ALU operating on a first upper portion of the first binary number and a second upper portion of the second binary number to produce a second result;

wherein at least one stage in the pipelined circuit stalls by one or more clock cycles in response to the carry out signal to account for additional delay introduced by incrementing the second result when the carry out signal indicates a carry.

19. (Original) The integrated circuit of claim 18, the pipelined circuit further comprising:

a first memory portion receiving the first result; and

a second memory portion receiving the second result.

20. (Original) The integrated circuit of claim 18, the pipelined circuit further comprising:

a logic circuit for incrementing a value stored in the second memory portion.

21. (Previously Presented) An integrated circuit comprising a pipelined arithmetic logic unit (ALU) operating on two binary numbers, the ALU comprising:

a first logic circuit generating a carry out signal from a bit location within the result of an operation on the two binary numbers;

wherein at least one stage in the pipelined circuit stalls by one or more clock cycles in response to the carry out signal to account for additional delay introduced by incrementing the second result when the carry out signal indicates a carry.

22. (Original) The integrated circuit of claim 18, the ALU further comprising:

a first logic unit operating on lower portions of the two binary numbers to produce a first result;

a second logic unit operating on upper portions of the two binary numbers to produce a second result;

a second logic circuit for incrementing the second result in response to the carry out signal to form an incremented value.

23. (Original) The integrated circuit of claim 18, the ALU further comprising:

a final result for the ALU is formed by combining:

the first result, and

selection of one of the second result and the incremented value, the selection being done in response to the carry out signal.

24. (Previously Presented) A method of operating on a first binary number and a second binary number, comprising:

adding a first lower portion of the first binary number and a second lower portion of the second binary number to produce a first result and a carry out signal; and

adding a first upper portion of the first binary number and a second upper portion of the second binary number to produce a second result; and

generating a pipeline stall signal in response to the carry out signal to cause at least one stage in a pipelined circuit to stall by one or more clock cycles to account for additional delay introduced by incrementing the second result when the carry out signal indicates a carry.

25. (Original) The method of claim 24 further comprising:
storing the first result in a first memory; and
storing the second result in a second memory.

26. (Original) The method of claim 25 further comprising:
incrementing a value stored in the second memory.

27. (Previously Presented) A method of operating on two binary numbers, comprising:

generating a carry out signal from a bit location within the result of an operation on the two binary numbers;

generating a pipeline stall signal in response to the carry out signal to cause at least one stage in a pipelined circuit to stall by one or more clock cycles to account for additional delay introduced by incrementing a portion of the result of the operation when the carry out signal indicates a carry.

28. (Original) The method of claim 27 further comprising:
operating on lower portions of the two binary numbers to produce a first result;
operating on upper portions of the two binary numbers to produce a second result;

incrementing the second result in response to the carry out signal to form an incremented value.

29. (Original) The method of claim 28 further comprising:

storing the first result; and

conditionally storing either the second result or the incremented value, the condition determined in response to the carry out signal.

30. (Cancel)

31. (Previously Presented) A processor, comprising:

at least first and second memory registers; and

a pipelined circuit apparatus for performing operations on first and second binary numbers stored in the first and second registers, comprising,

a first arithmetic logic unit (ALU) operating on a first lower portion of the first binary number and a second lower portion of the second binary number to produce a first result and a carry out signal, and

a second ALU operating on a first upper portion of the first binary number and a second upper portion of the second binary number to produce a second result,

wherein the pipelined circuit is configured to output a result of the operations performed on the first and second binary numbers at different pipelined clock cycles depending on the state of the carry out signal and to generate a stall signal to stall one or more stages of the pipelined circuit apparatus to account for a delay between the different pipelined clock cycles.

32. (Previously Presented) A pipelined circuit apparatus for performing operations on first and second binary numbers stored in the first and second registers, comprising:

a first arithmetic logic unit (ALU) operating on a first lower portion of the first binary number and a second lower portion of the second binary number to produce a first result and a carry out signal; and

a second ALU operating on a first upper portion of the first binary number and a second upper portion of the second binary number to produce a second result;

wherein the pipelined circuit is configured to output a result of the operations performed on the first and second binary numbers at different pipelined clock cycles depending on the state of the carry out signal and to generate a stall signal to stall one or more stages of the pipelined circuit apparatus to account for a delay between the different pipelined clock cycles.

33. (Previously Presented) A pipelined circuit apparatus for performing operations on first and second binary numbers stored in the first and second registers, comprising:

a first arithmetic logic unit (ALU) operating on a first lower portion of the first binary number and a second lower portion of the second binary number to produce a first result and a carry out signal;

a second ALU operating on a first upper portion of the first binary number and a second upper portion of the second binary number to produce a second result; and

a selection circuit for selecting, as the second result, one of the first upper portion and the second upper portion in response to at least one of first and second flag bits indicating whether a predetermined number of most significant bits of the first and second binary numbers, respectively, are all zero;

wherein the pipelined circuit is configured to output a result of the operations performed on the first and second binary numbers at different pipelined clock cycles depending on the state of the carry out signal and to generate a stall signal to stall one or more stages of the pipelined circuit apparatus to account for a delay between the different pipelined clock cycles.